Challenges and Opportunities in Advancing Metrology for Next-Generation Microelectronics

Tuesday, May 28, 2024, 10:30 a.m. – 12:00 p.m.

Chairs: Ran Tao (NIST) and Benson Chan (Binghamton University)

Moderator: Jan Vardaman (TechSearch International)

ECTC 2024 Special Session 2

Chair
Ran Tao
NIST

Chair
Benson Chan
Binghamton University

Moderator
Jan Vardaman
TechSearch International

Speaker/Panelist
Paul Hale
NIST

Speaker/Panelist
Gaurang Choksi
Intel Corporation

Speaker/Panelist
Zhihua Zou
TSMC

Speaker/Panelist
CP Hung
ASE

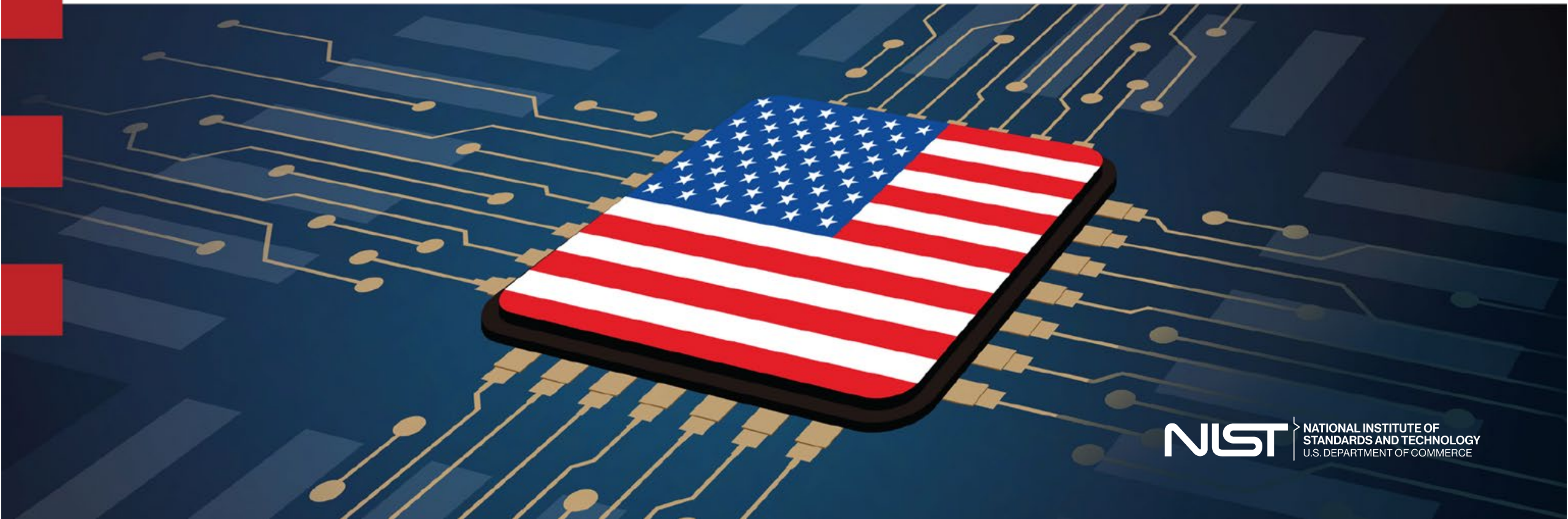
Speaker/Panelist
Chet Lenox
KLA Corporation

Challenges and Opportunities in Advancing Metrology for Next-Generation Microelectronics

Metrology plays a pivotal role in semiconductor research and manufacturing and is critical to the success of this industry. Advancements in measurement science, material characterization, instrumentation, testing, and manufacturing capabilities are critically needed to drive product innovation and ensure quality, yield, and manufacturing efficiency. During the panel discussion, experts will share their insights on the metrology challenges and opportunities that today's semiconductor industry is facing across every segment of the supply chain, with a focus on advanced semiconductor packaging for next-generation microelectronics (e.g., heterogeneous integration, wafer level packaging, hybrid bonding, etc.).

Advancing Measurement Science for Microelectronics: CHIPS Metrology Program

Paul Hale, Ph.D.
Deputy Director, CHIPS Metrology



Disclaimer

The purpose of this meeting is informational and preliminary only. It is not evaluative with regard to any applications or potential applications to the CHIPS Incentives Program. It is not part of the formal process of awarding funds. We are not authorized to make any commitments on any issues for the Department, including on specific questions on specific applicants.

We are holding these informational discussions with a broad set of individuals and organizations that have relevant knowledge for the CHIPS R&D Program. Nothing that we discuss should be understood as indicative or conclusive regarding the CHIPS Incentives Program.

Please do not share with us any information that you are required to keep confidential by law, contract, or professional obligation. NIST, CHIPS R&D, and the CHIPS Program Office does not seek and will not accept any material non-public information outside of a diligence process, which is separate from this meeting.

If you are currently serving a current or potential applicant to the CHIPS Program in any capacity that you feel could conflict with your participation, please inform us at any point in the discussion if there are topics you desire not to discuss or any other limitations on your participation that you desire.

Additionally, if you are aware of being directly and materially involved in an active procurement between your current organization and the U.S. Government, we would request to exclude any such topics from the discussion today.

CHIPS for America Programs

$39 billion
for manufacturing

Two component programs:

1. Attract large-scale investments in advanced technologies such as leading-edge logic and memory
2. Incentivize expansion of manufacturing capacity for mature and other types of semiconductors

$11 billion
for R&D

Four integrated programs to:

1. Conduct research and prototyping of advanced semiconductor technology
2. Strengthen semiconductor advanced test, assembly, and packaging
3. Enable advances in measurement science, standards, material characterization, instrumentation, testing, and manufacturing

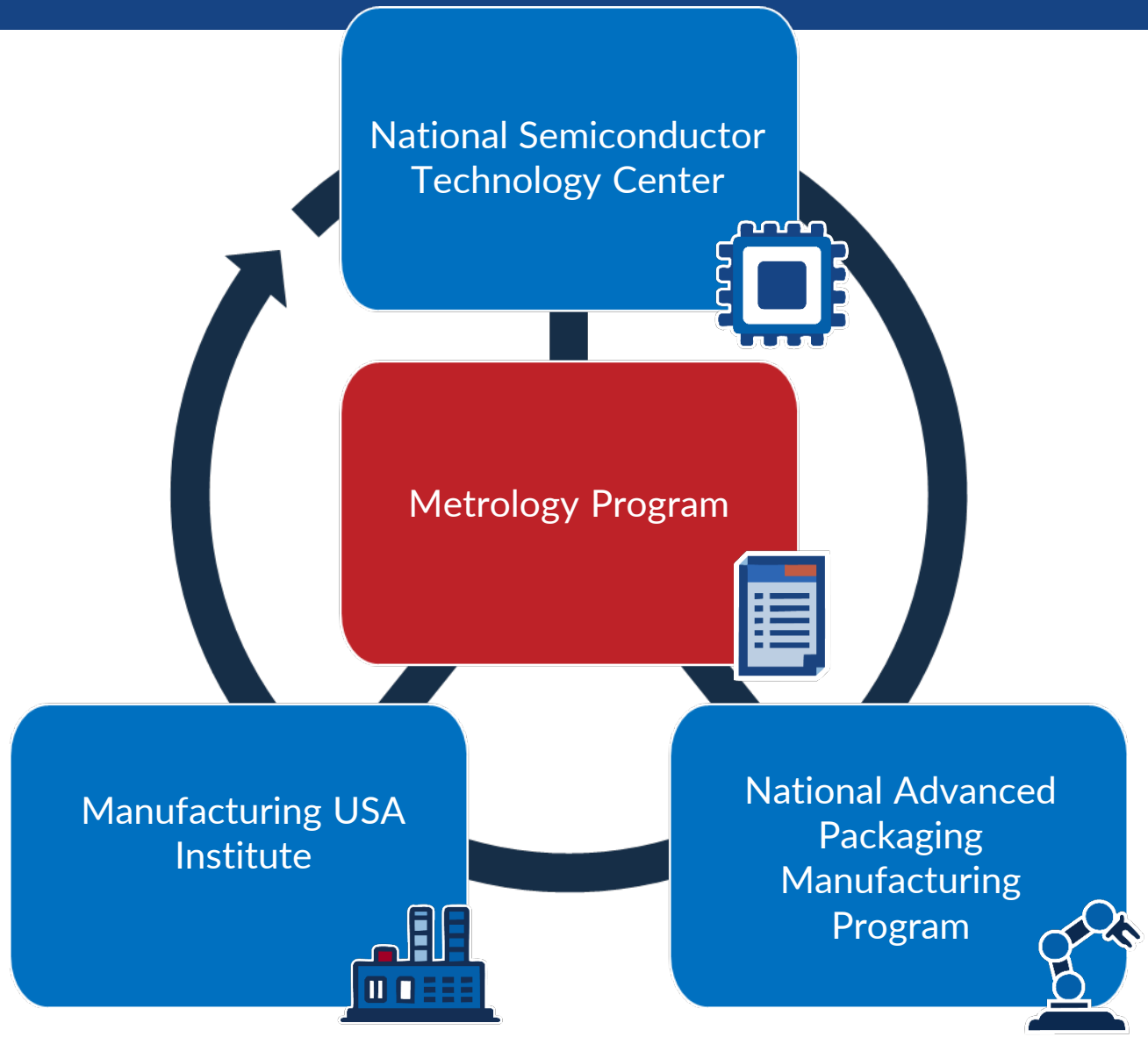
Together with CHIPS initiatives from other agencies, including DOD, State, NSF, and Treasury

CHIPS for America

To address gaps in the semiconductor ecosystem, CHIPS for America is investing in four overlapping entities, all of which include some aspect of workforce training.

These programs will share infrastructure, participants, and projects.

They will operate in coordination with each other, with the CHIPS for America manufacturing incentives program, and with microelectronics R&D programs supported by other U.S. federal agencies.



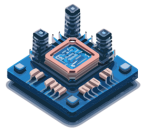
CHIPS Metrology Program Grand Challenges

CHIPS for AMERICA

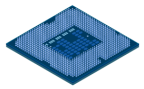
GC4 - Modeling and Simulating Semiconductor Materials, Devices, and Components

Design Metrology
Material and device models; physical metrology

Circuit and Package Design
Integrated circuits (IC), systems intregration



Mask Design
Template for the IC



GC1 - Materials Purity, Properties, and Provenance

Materials Quality Metrology
Acceptance inspection and testing for defects, purity, and other properties

Materials Supply
Over 800 diverse materials

GC5 - Modeling and Simulating Semiconductor Manufacturing Processes

Wafer Fabrication
Deposit a film, pattern a photoresist (litho), use as a stencil to etch the film

Deposition
Metal, dielectric

Lithography
Photoresist spin coat, expose, and develop

Etching
Heat/bake, etch, and remove resist

Repeat 40 –100 times

GC2 - Advanced Metrology for Future Manufacturing

In-line Fab Metrology
Inspection for defects; wafer and thin film quality inspection; mechanical testing; density and surface charge analysis; dimensional analysis of fine features

GC3 - Metrology for Advanced Packaging

Wafer/Package Metrology
Quality inspection; test for performance

Testing

Wafer Test
Each die individually tested on wafer

Packaging

Assembly/Integration
Wafer dice, sorting, die attach, bonding

Testing

Test Packages
Final product testing

End Products

Integration
Chips integrated in end products (OEMs)

Cross Cutting

GC6 - Standardizing New Materials, Processes, and Equipment

GC7 - Security and Provenance of Microelectric Components and Products

CHIPS Metrology: How far we've come

Grand Challenge Funded Research Projects

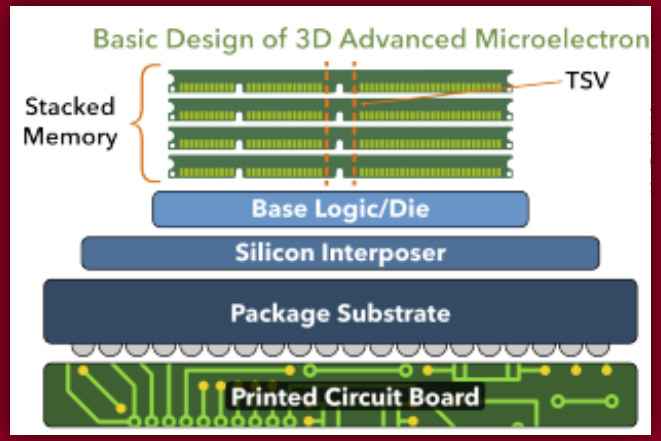
- Over **$109 million** in funding has been provided to **30 approved research projects** over three Grand Challenges
  - GC2 - Advanced Metrology for Future Microelectronics Manufacturing: **10 projects funded**
  - GC3 - Enabling Metrology for Integrating Components in Advanced Packaging: **7 projects funded**
  - GC4 - Modeling and Simulating Semiconductor Materials, Designs, and Components: **13 projects funded**
- Current projects are helping to develop new measurement instruments, measurement methods, and measurement-informed models and simulations for advanced microelectronics design and manufacturing.
- Additional projects will be selected by the end of the year

Industry & Academia Collaboration

- Research teams have proposed several distinct industry collaborators to provide materials and software and/or conduct joint research with researchers
- Several collaborations with U.S. universities, nonprofit consortiums, research institutes, and associations related to the microelectronics industries have also been proposed

Grand Challenge 3:

Enabling metrology for integrating components in advanced packaging



The Challenge: Provide enabling metrology that spans multiple length scales and physical properties and supports acceleration of advanced packaging concepts for future-generation microelectronics.

The Strategy: Develop metrology to enable complex integration of sophisticated components and novel materials for advanced microelectronics, strengthening the domestic semiconductor packaging industry and U.S. leadership in this critical sector.

The Path Forward: Conduct R&D to develop metrology to address the unique challenges presented by advanced packaging, including subsurface features and aspects related to heterogeneous integration and other innovative concepts. Critical areas include:

- Measurements for in situ, rapid measurements and verification methods for interfaces and subsurface interconnects, and internal 3D structures including warpage, voids, substrate yield, stresses, adhesion, and reliability with improved throughput and resolution.
- Physical properties (e.g., size, thermal, mechanical, electrical, magnetic, optical) for films, surfaces, buried features, and interfaces.
- Methods for integrating chiplets, dielets, SoCs, and memories into packages.
- Mechanical measurements for component integration (e.g., hybrid bonding and interfacial adhesion and bond integrity).
- Evaluation and correlation of data across the packaging process.
- Standards for packaging, such as reference materials and documentary standards, for areas including chiplets and SoCs.

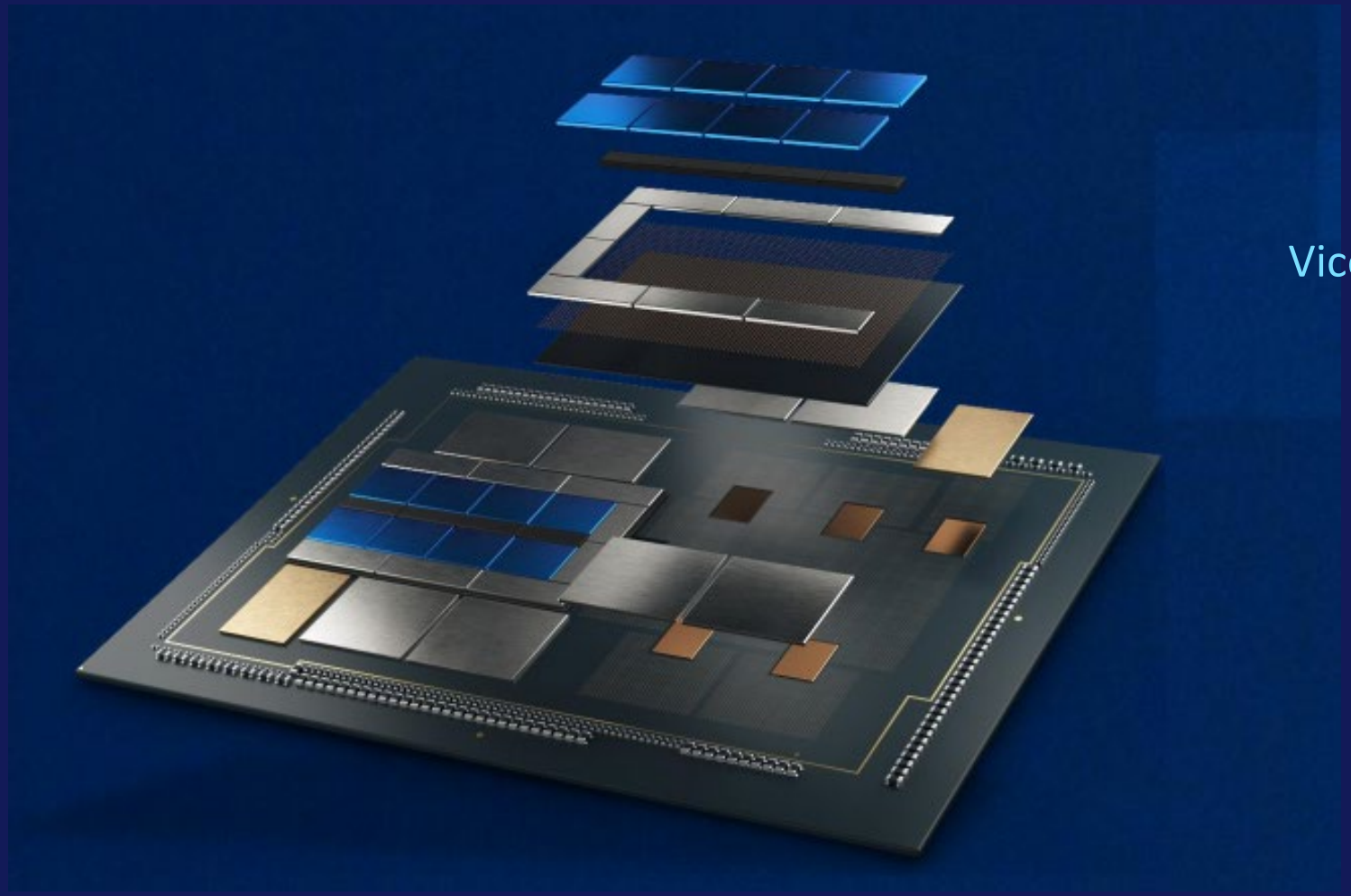
https://nvlpubs.nist.gov/nistpubs/CHIPS/NIST.CHIPS.1000.pdf

GC3 Funded Research Projects

Project Title	Summary
Accurate Cure Kinetics, Stress, Mechanical Properties and Warpage Measurements for Next-Generation Microelectronics Packaging under Device Relevant Conditions	Providing accurate measurements and tools for designing systems that focus on handling tight connections, smaller patterns, and increased layers, all while minimizing warping and maximizing thermal performance for long-lasting reliability, within a microchip.
Characterization of nano-to-microscale process-induced thermo-mechanical changes in heterogeneously integrated microelectronics	Develop and provide advanced measurement methodologies and data for addressing the thermal and mechanical challenges in the heterogeneous integration of modular chips in system-in-package manufacturing.
Metrology of Materials, Surfaces, and Processes for Hybrid Advanced Packaging	Applying NIST's analytical and metrological expertise to develop a scientific understanding of bonding processes in chiplet manufacturing, aiming to establish a predictive framework for efficient development of known good processes.
Metrology for Integration of New Magnetic Materials	Developing the necessary metrology, materials, and methods for integrating magnetic components with semiconductor materials, aiming to miniaturize and enhance the functionality of electromagnetic systems in fields like communications, radar, and advanced computation.
Nanoscale, Element-Specific X-ray Imaging for Integrated Circuit Metrology	Developing an advanced x-ray computed tomography instrument for 3D, element-sensitive imaging at micro to nano scales, enhancing subsurface feature characterization in integrated circuit (IC) chips for manufacturing and security, standardizing this technology for industry-wide 3D IC diagnostics.
Standardizing New Materials, Processes, and Equipment for Microelectronics - CalNet	Facilitating the measurement of S-parameters in integrated circuits by distributing research-grade on-wafer calibration kits and integrating NIST models into commercial software, culminating in a round robin evaluation.

Thank You

3D Heterogenous Integration
Metrology Challenges & Opportunities

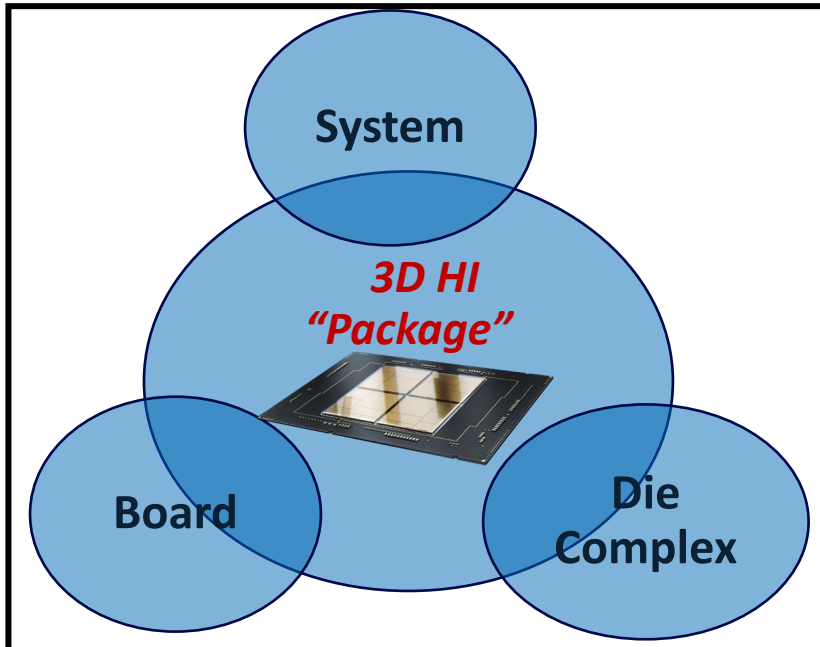


Gaurang Choksi
Vice-President, Foundry Technology Development
Intel Corporation

May 2024

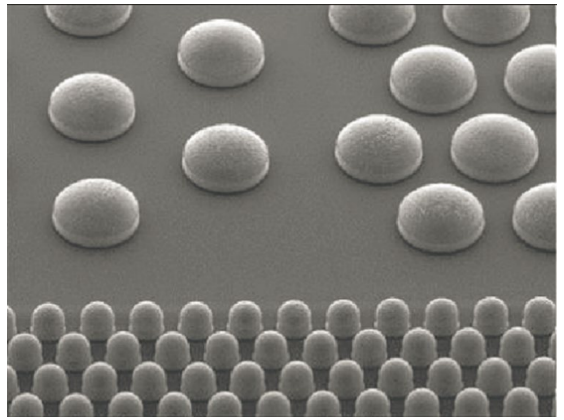
IEEE ELECTRONICS PACKAGING SOCIETY
ECTC
The 2024 IEEE 74th Electronic Components and Technology Conference

Moore's Law & Accelerating the Path to Zetta-Scale Computing

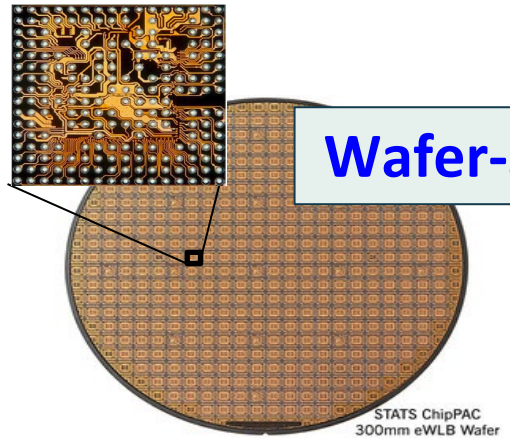


Blurring of the Interconnect Hierarchy

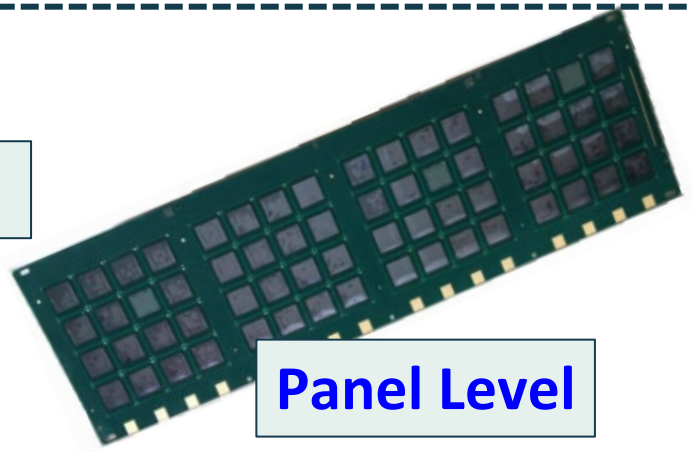
Architectures will evolve at the fastest pace in history!



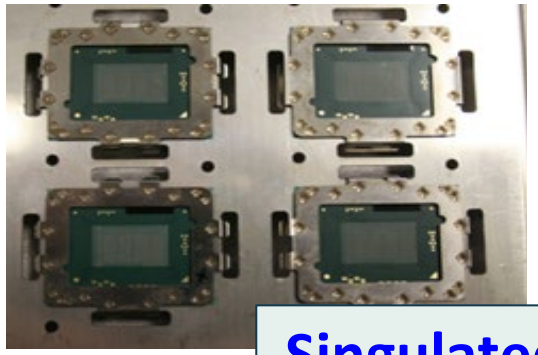
Pitch Scaling at ALL levels
('FLI', 'MLI', 'SLI')



Wafer-Scale



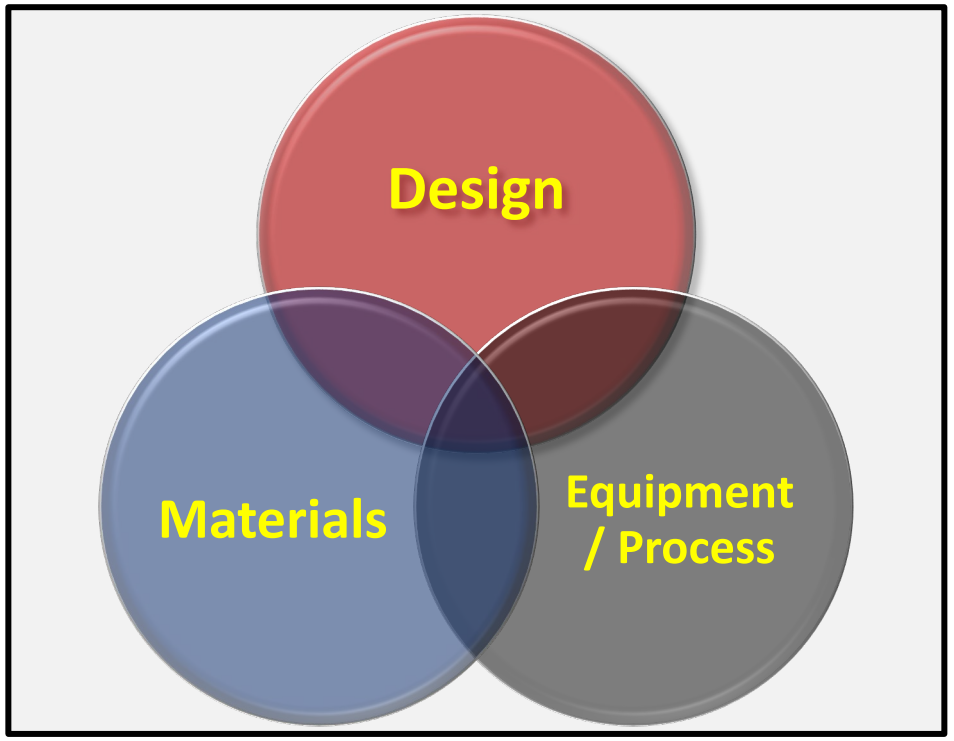
Panel Level



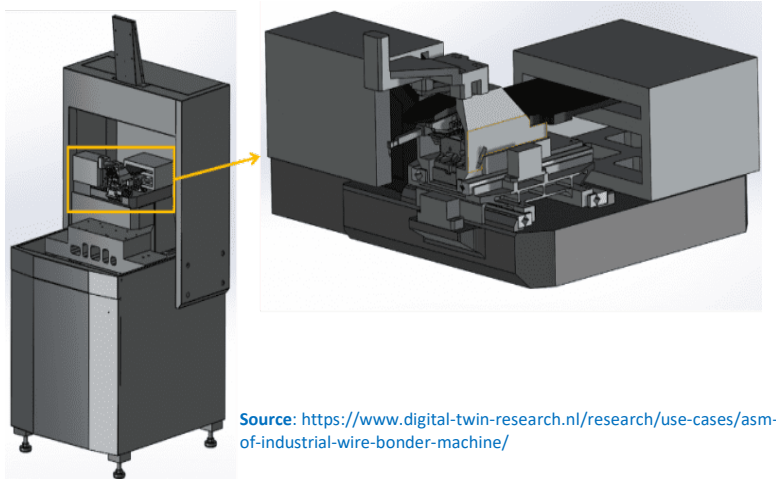
Singulated

Role of Integrated Sensors & Metrologies in Technology Development & Optimization

Lab Based Process Fundamentals



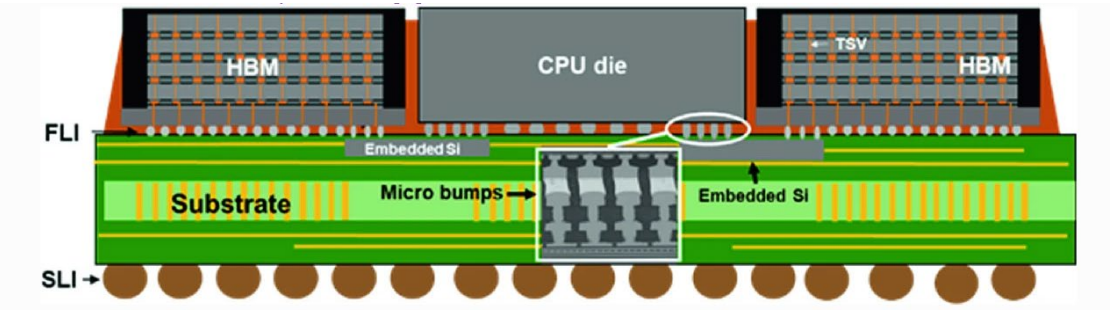
High Volume Manufacturing:
Sensor Integration for Process Development/Monitoring

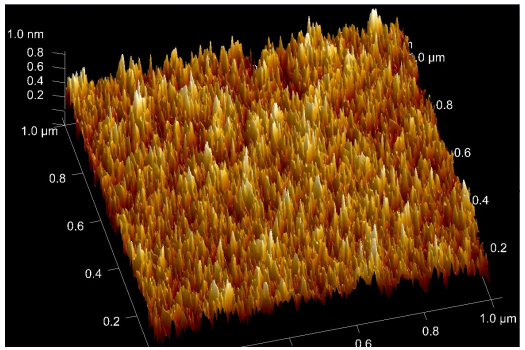


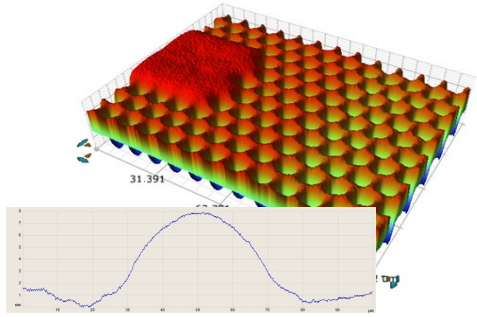
Role of Digital Twins

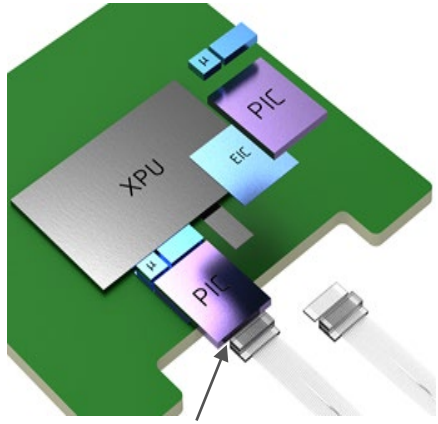
Source: https://www.digital-twin-research.nl/research/use-cases/asm-digital-twin-of-industrial-wire-bonder-machine/

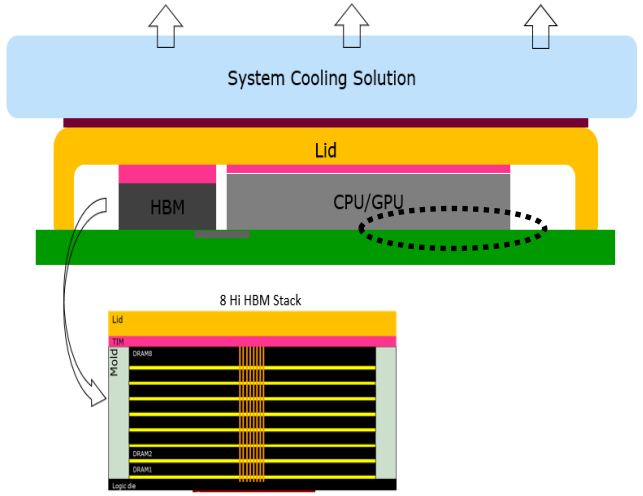
Scaling & Integration Demands on Metrologies: Examples

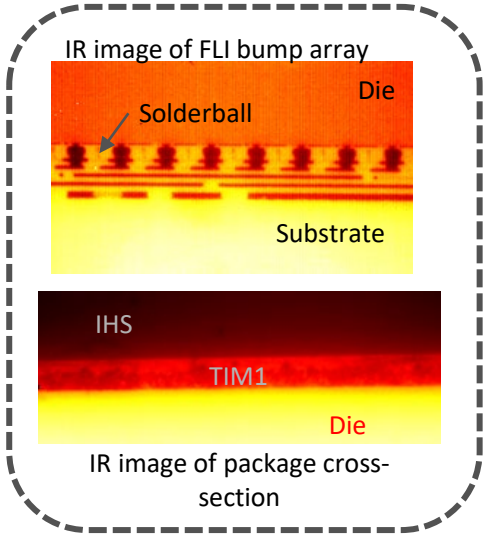












- Non-destructive imaging methods: Sub-um level crack detection
- In-line surface topology measurements: 0.1nm height & 1um X-Y resolution with <30s measurement time
- Roughness & flatness of deep trench vias / pillars
- 3D pad height / recess: ~1000X faster than AFM/WLI with 0.1nm vertical & 100nm lateral resolution
- Full field thermal imaging of structures beneath optically opaque layers; Accurate transient thermal metrologies

Need for Additional Standards

Dielectric Permittivity Standard Reference Material (SRM) - NIST/INEMI project

Frequency >10GHz, ideally spanning to 100GHz, Loss tangent <0.001

NIST traceable Dimension Standard at elevated temperatures

Step height ~3nm; Flatness standard; Temperature RT to 300 C

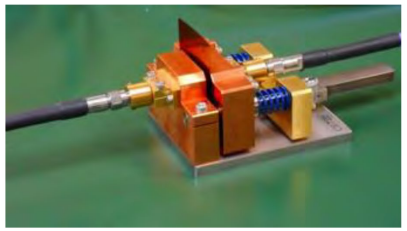
NIST NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
U.S. DEPARTMENT OF COMMERCE

Thermal Conductivity Reference Standards Development Survey

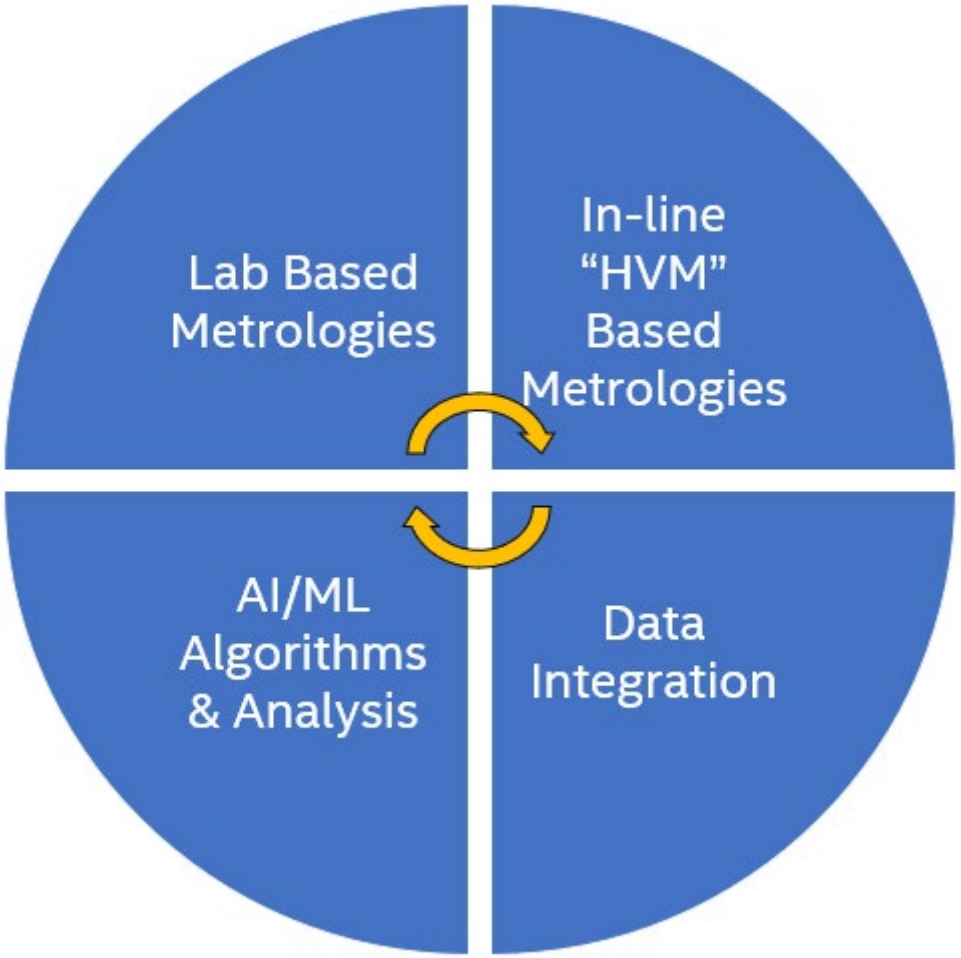
We are collecting information to guide the development of new Reference Materials (RMs)/Standard Reference Materials (SRMs) for thermal conductivity that will enable instrument validation, the reliable interlaboratory comparison of data, and ultimately accelerate the commercialization of materials and devices that rely on critical thermal property measurements. Feel free to forward the survey link to anyone you think has relevant needs and perspectives to contribute. Contact Joshua Martin (joshua.martin@nist.gov) with any questions. Thank you!

joshua.martin@nist.gov (not shared) Switch account

Thermal Conductivity Standard



Effectively Leveraging Metrology Data



***Challenge**: Amount of Data, Diversity of types of data & formats, Speed of access/processing*

Thank You

Unleash Innovation

Metrology for Advanced Packaging

Dr. Zhihua Zou
Advanced Packaging Technology Service, TSMC
May. 28th, 2024

TSMC 3DFabric™ Technology Portfolio

tsmc 3DFabric™

tsmc Unleash Innovation

3D Si Stacking

TSMC-SoIC®

- **SoIC-P (Bumped)**
  - CoW, Pitch: 16-25μm
- **SoIC-X (Bumpless)**
  - SoIC-X-C (CoW) Pitch: 3-9μm
  - SoIC-X-W (WoW) Pitch: < 3μm

SoIC: System on Integrated Chips

Advanced Packaging

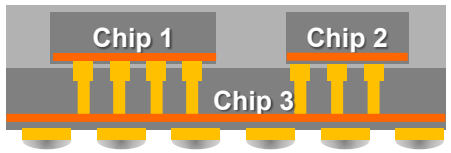
CoWoS®

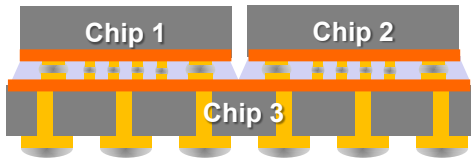
- **CoWoS-S (Si Interposer)**
- **CoWoS-L/R (RDL Interposer)**

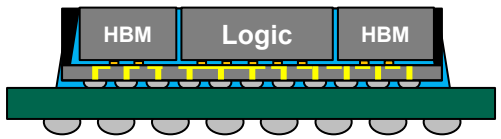
InFO

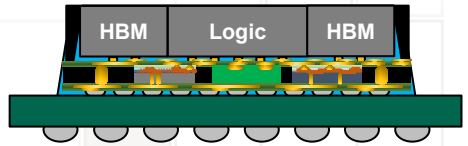
- **InFO-PoP**
- **InFO-2.5D/3D**

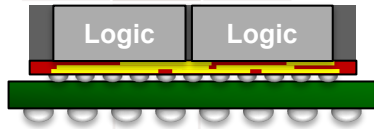
CoWoS: Chip on Wafer on Substrate
InFO: Integrated Fan-Out
PoP: Package on Package
RDL: Redistribution Layer



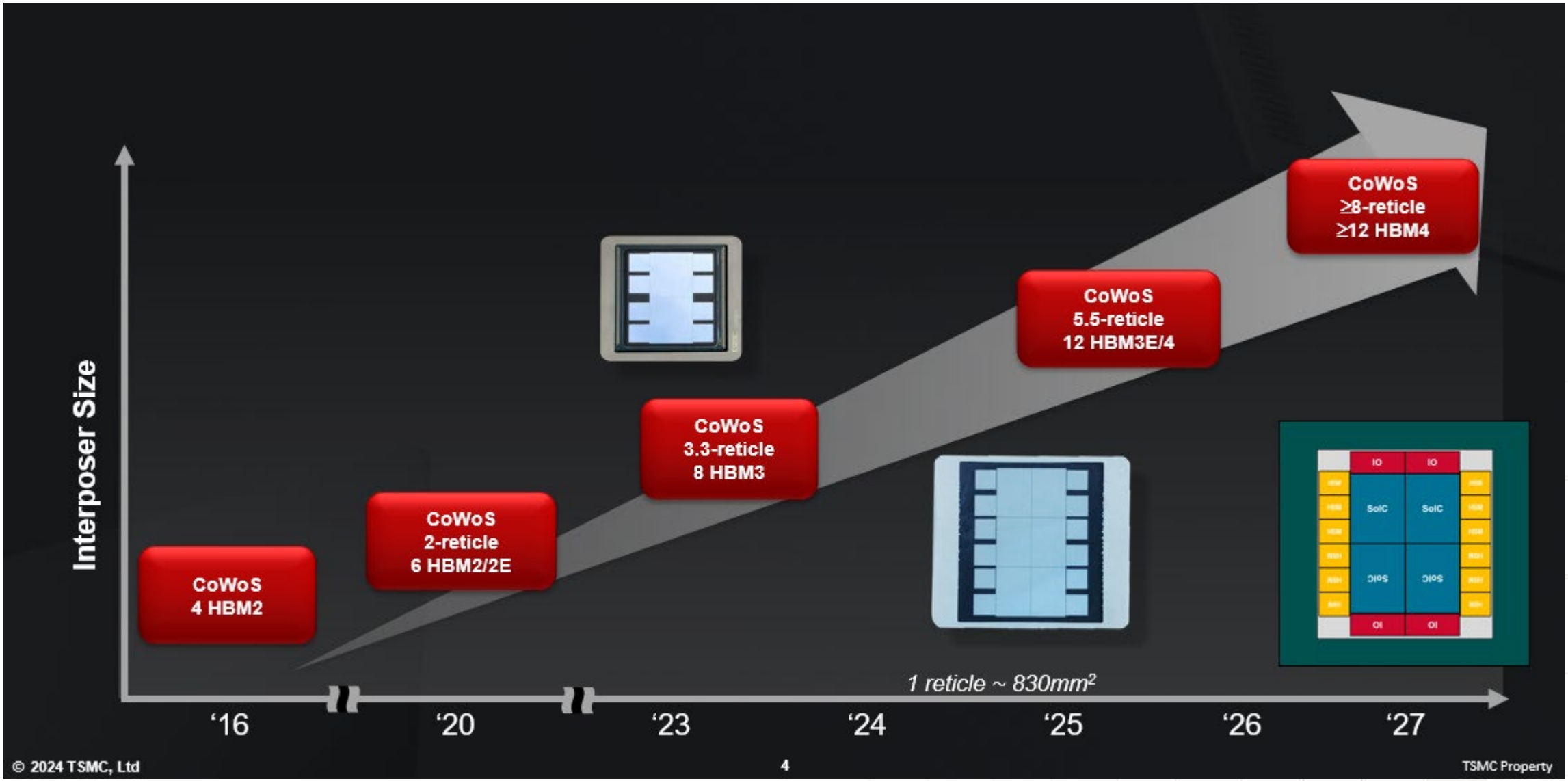




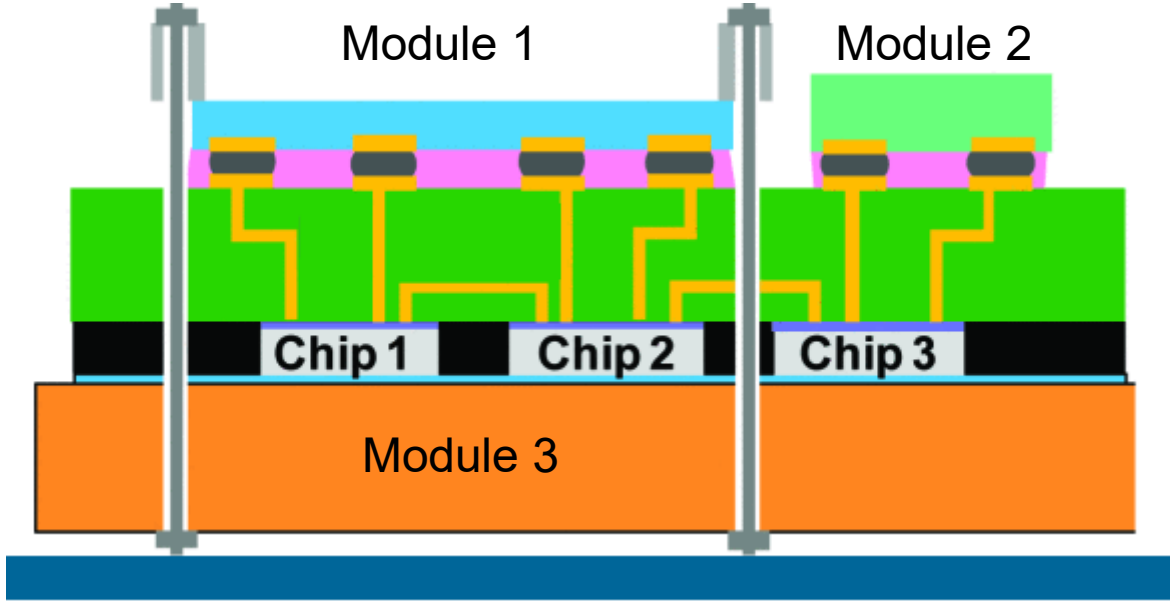


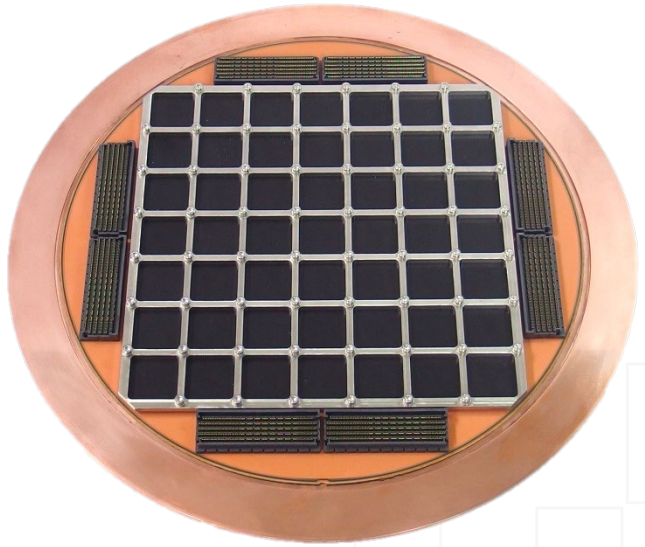


TSMC CoWoS® Integration



TSMC-SoW™ (System-on-Wafer)



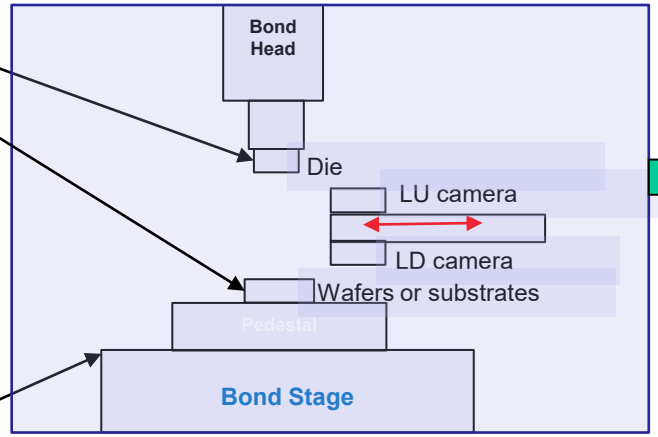


This SoW design posts significant challenges from defect inspection point of views from the algorithms and memory point of view comparing to other packaging.

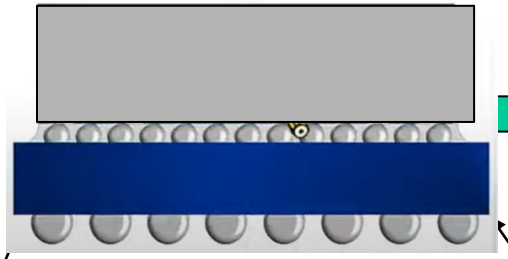
Metrology plays big role at each stage of processes and whole process flow

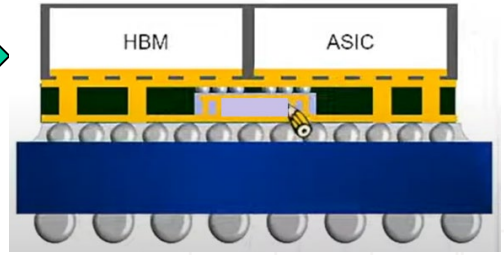
Incoming material/parts quality control /characterization metrology:
Dies/wafers/pedestal, etc.

Quality Assurance, reliability, failure analysis metrology for final products



bonding tool schematic





In-situ metrology to monitor the process health such as bonding force, temperature, part quality check? Post bonding time zero alignment?

In-line metrology to monitor the product performance just after the process: alignment, visual, warpage, etc?

Offline metrology to characterize the process/ product performance: X-ray, IR, CSAM, profiler, etc?

Metrology Trends for Advanced Packaging

Unleash Innovation

- **The boundary of FE and BE metrology becomes more mixed plus BE have different challenges.**
  - Lateral CD measurement precision needs to be 10nm level
  - Vertical CD measurement in SoIC needs to be 0.1nm level.

- **Lab tools vs. Mass Production Tools**
  - More demands to make lab tools to be applied on mass productions.
  - Tool to tool matching from inputs/parts/outputs are critical for mass productions

- **High Wafer Warpage handling capability Needed**.
  - 1500um → 3000um → 4000um level of wafer warpage

- **Large Data Process capability**
  - 1B bumps per wafer expected
  - How to do defect inspections for large dies (6X or SOW type of wafers) with high resolutions: 2T pixel level data processing
  - Machine Learning needs to be built in

- **Inner defect detection capability needs significant improvements or technology breakthrough**

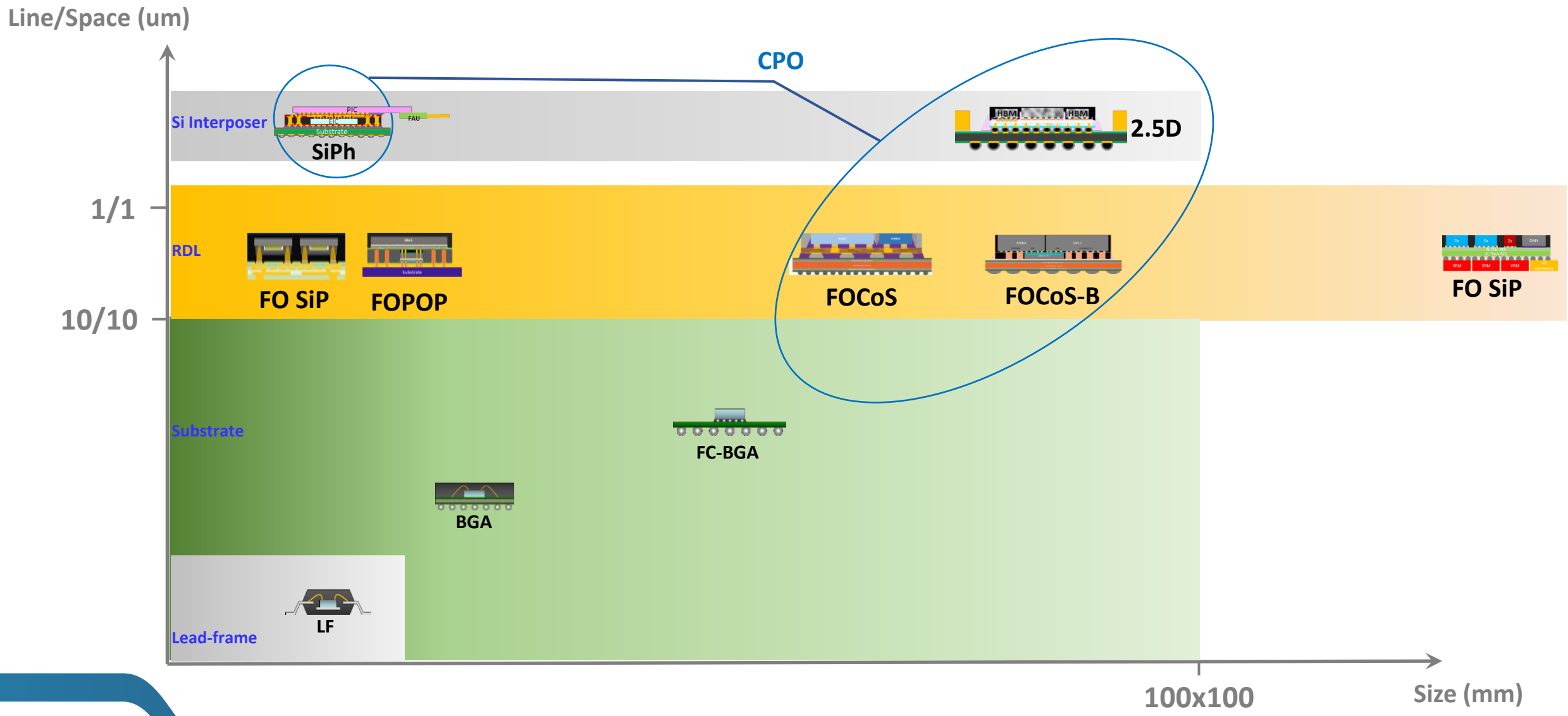
Thank You!

CP Hung, Ph.D.

Vice President of Corporate R&D, ASE Group

IEEE EPS Board of Governor; SEMICON Taiwan PKG & TEST Committee Co-Chair

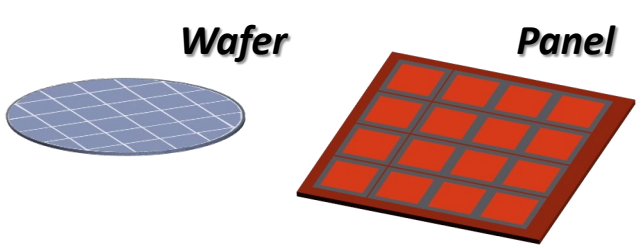
Advanced Packaging Solution

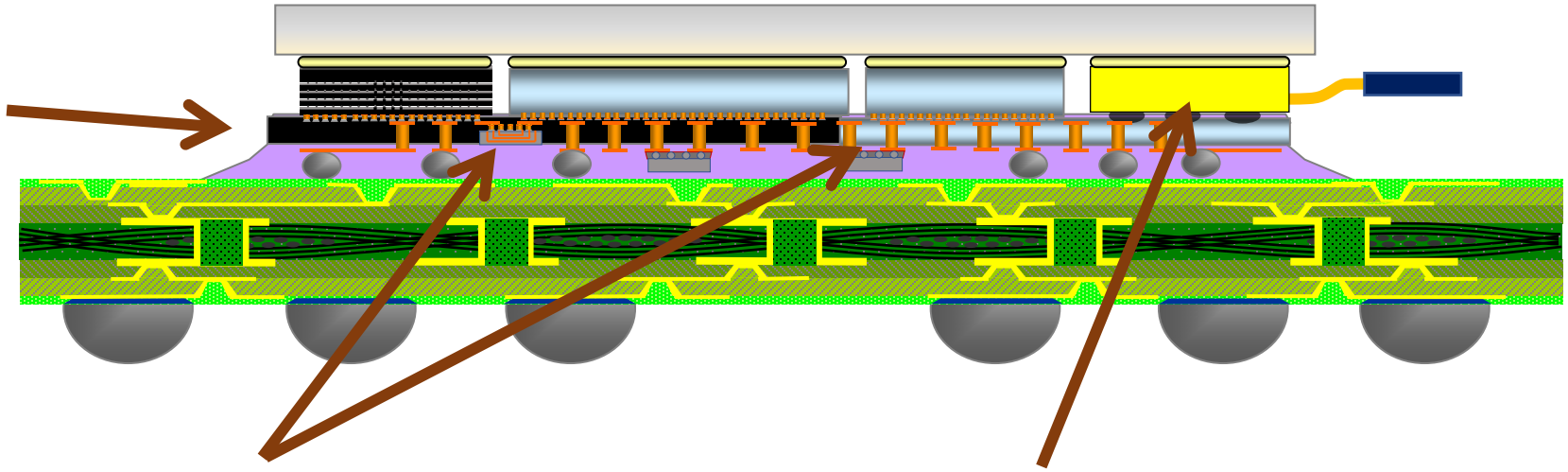


Metrology Outlook for Advanced Packaging

Comprehensive Structures for Heterogeneous Integration

- Ultra High Density Fine Pitch L/S & Bonding
- Complex Interconnection and Combo Platforms Structure





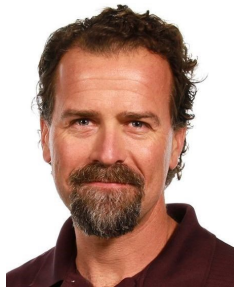
Advanced Metrology Inspection & Analysis

- Electrical, Thermal, Stress & Reliability
- Material/Chemical Characterization & Simulation
- e-FA, Nondestructive Inspection & p-FA
- Metal Composition, EM, Surface & Morphology Inspection

In-Process Inspection & Critical Measurement

- Electrical and Optical interconnection
- 2D and 3D Defect Detection and Measurement
- Multi-sensing/Full Automation in Smart Manufacturing
- ML / AI assisted Inspection Integrated Diagnosis

Thank You



Chet Lenox, Ph.D.

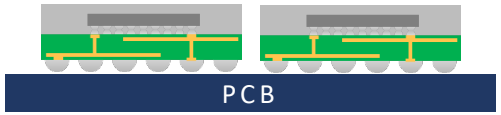
Fellow, Industry and Customer Collaboration, KLA

Process Control in Advanced Packaging

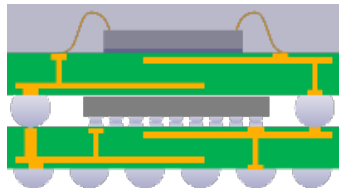
- Heterogeneous integration in packaging is not new, but evolving quickly
- More companies bringing front-end technologies to packaging

1D on-board | 2D package-level | 2.5D chip-level | 3D chip-level

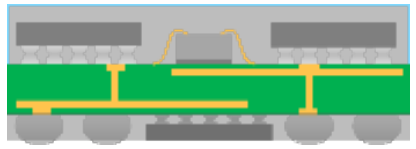
logic memory



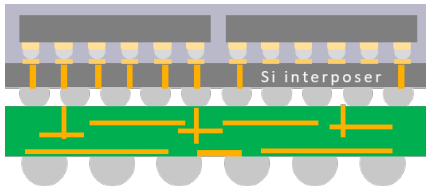
package on package (POP)



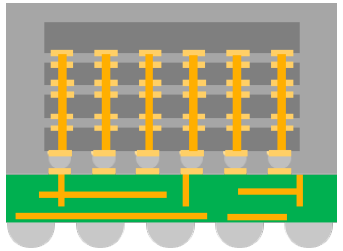
system in package (SiP)



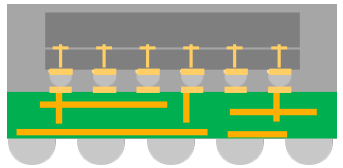
Si interposer and TSVs



memory stacking

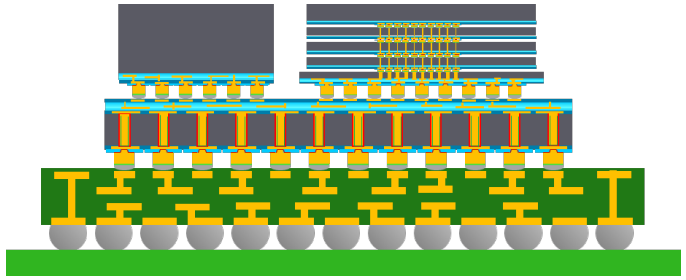


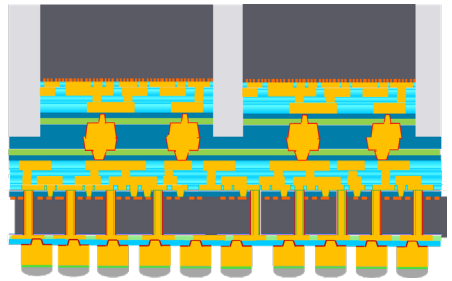
logic stacking



More wafer-level processes, complex assembly, smaller features, higher value

2.5D and 3D Packaging Process Control



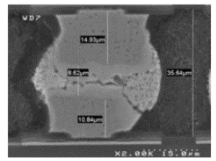


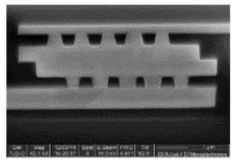
	2.5D Processes	3D Processes
Inspection	▪ TSV bottom defectivity ▪ RDL pattern/surface defectivity	▪ Bonding surface defectivity ▪ Post-assembly defectivity
Metrology	▪ Wafer thinning thickness ▪ TSV profile and depth ▪ Via reveal height ▪ RDL CD and height ▪ Plating chemistry	▪ Wafer thinning ▪ Oxide gap fill profile ▪ Bonding surface profile ▪ Wafer and die warpage ▪ Chiplet bonding alignment

Key focus areas for KLA
(not an exhaustive list!)

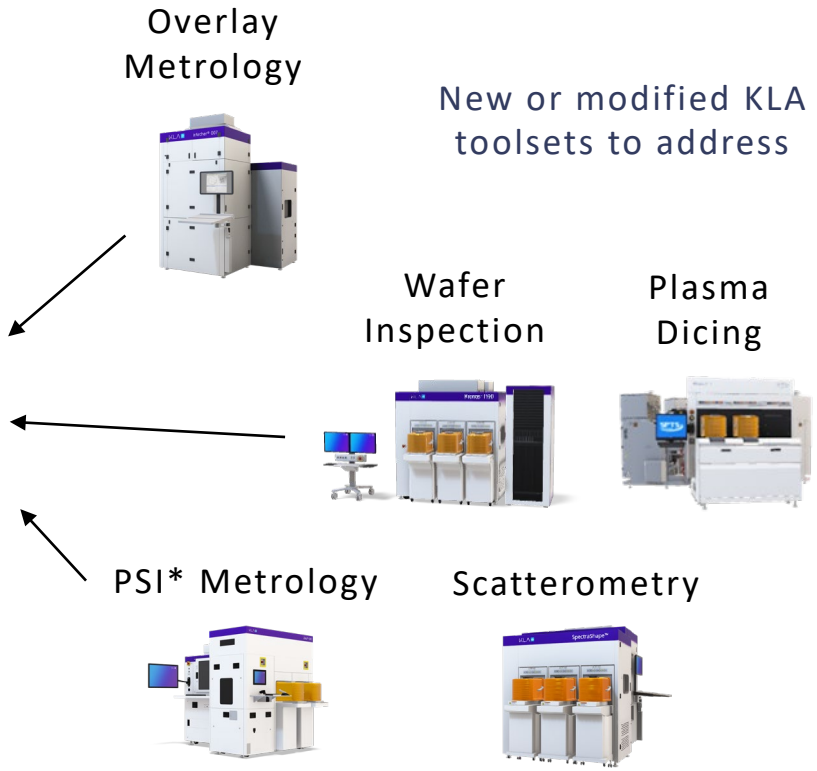
One Example: Hybrid Bonding

- Higher sensitivity inspection
- Higher precision and new features in metrology





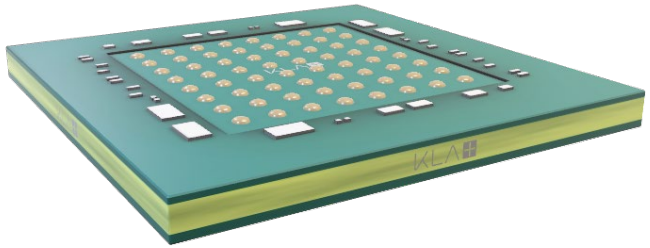
Requirement	uBump	Hybrid Bonding
Bonding Alignment Accuracy	~3-10µm	<0.3µm
Bonding Interface Defects	Microns	Sub-micron
Surface Topography	µm	nm
Patterning Method	Aligner/I-Line	248nm Scanner
Die Warpage	~60-100µm	10-20µm



Reference: uBump and HB requirements as outlined by Marvin Liao, ISES AP Summit, May '21
**PSI = phase shift interferometry*

Inspection and Metrology for IC Substrates

- IC substrate evolution
  - Larger body, finer line/space, thinner laminates, embedded features
- IC substrate innovation driving inspection and metrology requirements
- Glass core and panel-format interposers on carriers bringing entirely new challenges



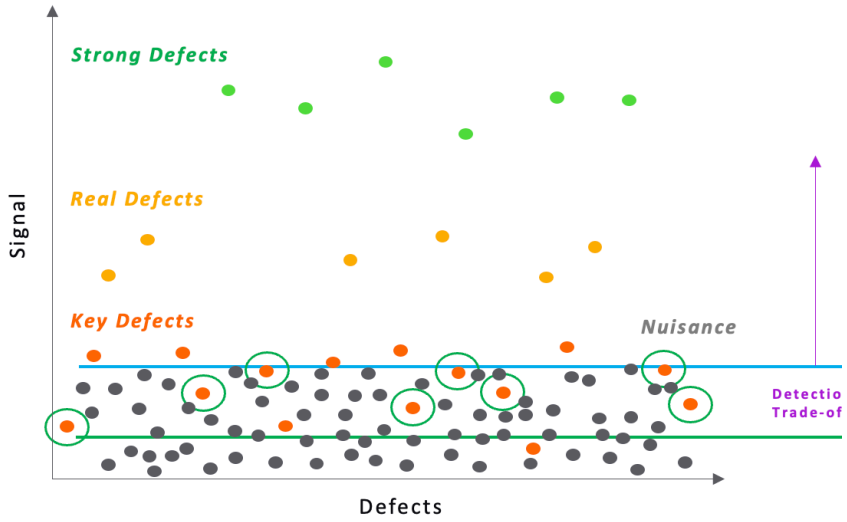
	Challenges
Inspection	▪ Sensitivity to smaller defects ▪ Capture rate ▪ Corrosion noise sources ▪ Post-singulated inspection
Metrology	▪ Step height and critical dimensions ▪ ABF film thickness ▪ Topography and warpage

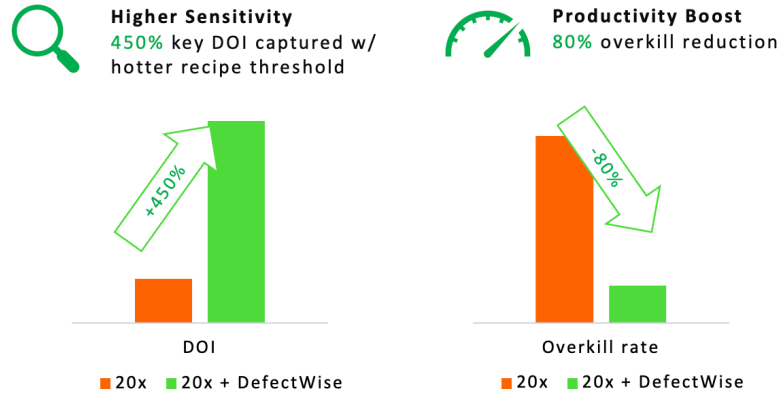
AI Algorithms in Process Control

- AI has been a key algorithm technology in defect inspection for many years
- Nuisance reduction, defect classification, screening, metrology precision, and more

First KLA system with integrated AI (2020):
eSL10™ e-beam defect inspection

Application of Run-time, Image-based Deep Learning for Defect Thresholding*





*KLA's Kronos™ wafer-level inspection system applied to RDL patterning

Thank You

Panel Discussion:
Challenges and Opportunities in Advancing Metrology for Next-Generation Microelectronics

Moderator: **Jan Vardaman** (TechSearch International)

Panelists:

- **Paul Hale** (NIST)
- **Gaurang Choksi** (Intel)
- **Zhihua Zou** (TSMC)
- **CP Hung** (ASE Group)
- **Chet Lenox** (KLA)